Remarks

Claims 1, 4-5, 7-8, 10, 12-13, 16, 18-19, and 21-27 are pending in this action. Claims 1, 4-5, 7-8, 10, 12-13, 16, 18-19 stand rejected. Claims 21-27 are subject to a restriction requirement. By this amendment claims 1, 4-5, 7, 10, and 16 have been amended, and claims 21 – 27 have been withdrawn. Applicants respectfully request reconsideration of all pending claims herein. No new matter has been added to the application by virtue of the present amendment.

Restriction Requirement

The Office Action stated that newly submitted claims 21-27 are directed to an independent or distinct invention. Therefore, Applicant elects claims 1, 4-5, 7-8, 10, 12-13, 16, 18-19, and request that claims 21-27 be withdrawn from consideration.

Claim Objections

Applicants respectfully submit that the amendments to claims 1, 4-5, 7, 10, and 16 more clearly define and claim Applicants' invention as suggested by the final Office Action mailed 02/06/06 (see pgs. 5-6, and 11). Amendments to claims 1, 10, and 16 specifically point out the limitation of "integrated circuit details are hidden from the user" is analogous to using a "black box circuit", and is adequately described in Applicants' specification (see Lehner Abstract, paragraphs 10-12, 57, 89, 102).

Applicants have amended claims 4-5, and 7 to comply with the statutory category of the claim from which they depend (a computerized simulation system apparatus) as suggested in the Office Action (see pg. 5). Applicants' have further amended claim 1 to more clearly define the invention and remove ambiguous language as suggested in the Office Action (see pg. 5-6). With regards to claims 4-5 (see pg. 6 of the Final Office Action) Applicants' submit that amended

claims 4-5, which recite a "including a static load model" and "including a dynamic callback function which defines the load parameters" respectively, more clearly define Applicants' invention and are adequately described in the context of Applicants' specification and the knowledge of one of ordinary skill in the art (see Lehner paragraphs 25, 77-78, 81, 87). Claims 10 and 16 have been amended to clearly differentiate the terms "modeling" and "simulating" (see Office Action pg. 6).

Claim Rejections - 35 U.S.C. § 101

The Office Action stated that claims 1, 4-5, 7-8, 10, and 12-13 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Applicant has amended 1, 4-5, and 7-8 to specifically claim statutory subject matter in the form of a computerized simulation system that includes a *tangible* computer system (see Lehner Fig. 8), a *tangible* integrated circuit design to be simulated (inherent in the invention), and a *tangible* black box circuit model (see Lehner Figures 3-5) used to perform the useful art of circuit simulation. The black box circuit model is tangible because it can be built in hardware using basic electrical components including resistors, capacitors, diodes, transistors and other basic circuit elements. The "simulator module", "code module", and "interface" are tangibly embodied in the computer system as machine readable code. Applicants submit that machine readable code is inherent in all computer systems.

Applicant has amended claims 10 and 12-13 to specifically produce the tangible result – the result being a fully simulated circuit (as discussed in an interview with the Examiner on 3/28/06) and thus be in compliance with the rules established in MPEP 2106(II)(A).

Applicants respectfully submit that based on the foregoing arguments and amendments,

the 35 U.S.C. 101 rejection of claims 1, 4-5, 7-8, 10, and 12-13 has been overcome.

Claim Rejections - 35 U.S.C. § 103(a)

The Office Action stated that the Application currently names joint inventors (Office Action pg. 9). Applicants respectfully request clarification as to which other Application the Examiner is referring to.

The Office Action stated that claims 1 – 20 are rejected under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent No. 6,077,304 issued to Kasuya (Kasuya) in view of "How Computers Work, 6th Edition" by Ron White (White), further in view of "IEEE 100 The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition" (IEEE), further in view of "Microsoft Computer Dictionary, Fifth edition" (Microsoft). The Office Aciton stated that Kasuya discloses a circuit simulator implemented on a computer system including a user interface and an API to control the simulator. The Examiner further stated that White and Microsoft disclose concepts such as dynamic link libraries and that IEEE discloses definitions for APIs.

Applicants submit that Kasuya does not teach a means for ***both "secretly" modeling*** a circuit as a black box ***and precisely simulating*** the original circuit using the black box circuit. Kasuya discloses an abstracted model, which cannot be simulated with precise accuracy (see Kasuya Col. 1 lines 47-56), and further, Kasuya's method of providing precisely accurate circuit simulations requires access to circuit details using netlists which specify the nature of its components (see Kasuya Col.1 lines 29-46, Col. 4, lines 32-45). The simulation engine described by Kasuya uses ***predefined*** circuit models 116 (i.e. detailed transistor-level models), which are used to represent ***specific circuit components*** and the models are stored in a library (see Kasuya

col. 4 lines 25-34). The abstracted models and detailed transistor-level models described by Kasuya, 1. cannot be simulated simultaneously using Kasyua's disclosed method, and 2. cannot provide an accurate simulation result while hiding circuit details. Furthermore, the simulation method described by Kasuya cannot be combined with any of the other references cited, to create Applicant's claimed invention because none of the other references teach a method of modeling and simulating a black box circuit with the accuracy and precision of a transistor-level model. Applicants' invention both models a circuit as a black box and precisely simulates the black box circuit in such a way that neither the user nor the simulator has access to the circuit details at any point during the simulation. (See Lehner Abstract, Summary, Paragraphs 8-11, 89, 102, Fig. 7, amended claims 1, 7, 10 and 16).

The invention disclosed by Kasuya does not include a circuit module or a simulation module as described in the instant application (see Lehner Fig. 8, amended claims 1, 10, and 16) both of which are key elements of the present invention. Furthermore, none of the other references cited describe a simulation module or a circuit module as described in the instant application. In Kasuya's disclosed invention, the simulator is not hidden from either the simulation verification sub-system 104, or the user via user interface 114 (see Kasuya, Col. 4, lines 26-32).

Another difference is that in the system described by Kasuya the user sends inputs directly to the circuit simulator and the circuit simulator calls the models (see Kasuya figure 1). Figure 1 of Kasuya shows the main verification subsystem calling the simulator API, thus the program makes direct calls to the simulator which in turn calls the models. In the instant Application, the circuit module calls the simulator module rather than the simulator module calling the circuit module (see Lehner Fig. 8). Furthermore, the user described in the instant Application does not provide inputs directly to the API simulator. The user supplies inputs only to the code module,

which in turn calls the API simulator to reproduce the black box circuit model's behavior (see amended claims 1, 10, and 16 herein).

None of the references when combined with Kasuya teach or motivate one of ordinary skill in the art to create an accurate circuit model whose circuit details are hidden from the user and the circuit simulator.

Applicants have amended claims 1, 4-5, 7, 10, and 16 to clarify the claimed invention, as noted above, and thus patentably distinguish it from the references cited by the Examiner. Accordingly, Applicants respectfully submit that the rejection of claims 1, 4-5, 7-8, 10, 12-13, 16, and 18-19 under 35 U.S.C. § 103(a) has been overcome and all claims are in condition for allowance.

Summary and Conclusion

Based on the foregoing, it is respectfully submitted that the pending claims in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
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